CLAIMS

1. A data processing circuit comprising at least a first functional unit (304) able to perform a n-taps polyphase filtering and a second functional unit (306) able to perform a m-taps polyphase filtering, m and n being integers greater than or equal to two, as well as a memory device (301, 302, 308) able to store data and coefficients, characterized in that the functional units are able to receive in parallel data and coefficients coming from the memory device, calculate results from said data and coefficients and supply these results to the memory device.

2. A processing circuit as claimed in Claim 1, characterized in that at least one functional unit is able to function according to a direct mode and a transposed mode, the circuit comprising control means (511-514) for controlling the functioning mode of said functional unit.

3. A processing circuit as claimed in one of Claims 1 and 2, characterized in that at least one functional unit is also able to perform a multiplication-accumulation using two data items coming from the memory device.

4. A processing circuit as claimed in any one of Claims 1 to 3, characterized in that it comprises a crossbar (303, 307) able to perform a transfer of data, coefficients and results between the memory device and at least one functional unit.

5. An image processing system comprising a processing circuit as claimed in Claim 1.

6. A receiver decoder device for television comprising at least one image processing system as claimed in Claim 5.

7. A device comprising at least one screen intended to display images and an image processing system as claimed in Claim 5.

8. A communication network comprising at least one transmitter able to send signals representing at least one image, a transmission network, a receiver able to receive said signals and an image processing system as claimed in Claim 5.